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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,826	05/29/2007	Masaaki Kanasugi	5053-2	6806

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EXAMINER	
PARVEZ, AZM A	
ART UNIT	PAPER NUMBER
4136	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,826	KANASUGI ET AL.	
	Examiner	Art Unit	
	AZM PARVEZ	4136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim1-3,5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuramitsu et al., JP 2001044064 , in view of Kobayshi et al.,JP 2002343674 and further in view of Tokuoka et al., US 6550117.

4. Regarding claim 1 , Kuramitsu et al. disclose:

A process for producing a multilayer (see Kuramitsu et al. Fig 3 d) **for a multilayer electronic device, comprising a dielectric layer of a ceramic**

green sheet (see Kuramitsu et al.13; Fig 2b)**, an adhesive layer, an electrode layer** (see Kuramitsu et al. 12; Fig 1b) **with a predetermined pattern and a spacer layer with a complementary pattern of the predetermined pattern, which electrode layer and spacer layer are laminated on an upper surface of the dielectric layer through the adhesive layer, using (I) an electrode layer-forming roll (1) obtained by winding up an electrode sheet (10) having a layer structure comprising a first substrate sheet (11) and an electrode-spacer layer (14) into a roll shape** (see Kuramitsu et al. Para7; Detailed Description) **; (II) an adhesive layer-forming roll (2) obtained by winding up an adhesive layer-forming sheet (20) having a layer structure comprising a back transfer (offset)-preventing layer (21)** (see Kuramitsu et al. Para35; Detailed Description) **, a second substrate sheet (22) and the adhesive layer (24) into a roll shape; and (III) a green sheet roll (3) obtained by winding up the ceramic green sheet (30) having a layer structure comprising a third substrate sheet (31) and the dielectric layer (33) into a roll shape**(see Kuramitsu et al. Para7; Detailed Description) **, said process comprising: (A) a first step of transferring only the adhesive layer (24) of the adhesive layer-forming sheet (20) wound off from the adhesive layer-forming roll (2) onto an upper surface of the electrode-spacer layer (14) of the electrode sheet (10), while winding off the electrode sheet (10) from the electrode layer-forming roll (1); (B) a second step of transferring only the dielectric layer (33) of the ceramic green sheet (30) wound off from the green sheet roll (3) onto the adhesive layer (24) transferred onto the upper surface of the**

electrode sheet (10) (see Kuramitsu et al.Para30; Detailed Description & Fig 3) **delivered from the first transfer step; (C) a third step of bonding the adhesive layer-forming sheet (20) wound off from the adhesive layer-forming roll (2) onto the dielectric layer (33) transferred onto the upper surface of the electrode sheet (10) delivered from the second transfer step, through the adhesive layer (24) of the adhesive layer-forming sheet (20), thereby forming a multilayer sheet (40)** (see Kuramitsu et al.Para30; Detailed Description &Fig 3) **; and (D) a fourth step of winding up the multilayer sheet (40) delivered from the third step, thereby producing a multilayer sheet roll (4)** (see Kuramitsu et al.Para31; Detailed Description & Fig 3) .

Kuramitsu et al fail to disclose **an adhesive layer, (A) a first step of transferring only the adhesive layer (24) of the adhesive layer-forming sheet (20) wound off from the adhesive layer-forming roll (2) onto an upper surface of the electrode-spacer layer (14) of the electrode sheet (10), while winding off the electrode sheet (10) from the electrode layer-forming roll (1);**

However, Kobayashi et al., JP 2002-343674 disclose:

[O027]Next, as shown in drawing 6 and drawing 7, the electrode paste of the internal electrode 18 which makes nickel the main ingredients at a layered product is screen-stenciled on the upper surface of said lower invalid layer 20, After drying, said green sheet 14 laminated via the ** form agent layer 12 and the binder layer 15 on the carrier film 13 was stuck by pressure, it exfoliated from the

interface of the account ** type agent layer 12 of back to front and binder layer 15, and the one green sheet 14 was laminated.

It would have been obvious to one with ordinary skill in the art at the time of invention to binding electrode layer with dielectric layer using adhesive layer for reliable multilayer structure with high adhesive strength to avoid thermal crack as taught by Kobayshi et al.

Kuramitsu et al. together with Kobayashi et al. fail to disclose **a spacer layer with a complementary pattern of the predetermined pattern, which electrode layer and spacer layer are laminated on an upper surface of the dielectric layer.**

However, Tokuoka et al. disclose in column 6 paragraph 4:

As shown in FIG. 2A, green internal electrode portions 22 are disposed on a green dielectric layer 21. Moreover, green dielectric portions 23 are disposed to bridge gaps among the green internal electrode portions 22.

It would have been obvious to one with ordinary skill in the art at the time of invention to make electrode spacer layer by forming complimentary pattern for precise flattened surface to avoid piercing of dielectric layer as taught by Tokuoka et al.

5. Regarding claim 2 , Kuramitsu et al. disclose:

A process for producing a multilayer (see Kuramitsu et al. Fig 3 d) **for a multilayer electronic device, comprising a dielectric layer of a ceramic green sheet** (see Kuramitsu et al.13; Fig 2b)**, an adhesive layer, an electrode**

layer (see Kuramitsu et al. 12; Fig 1b) **with a predetermined pattern and a spacer layer with a complementary pattern of the predetermined pattern, which electrode layer and spacer layer are laminated on an upper surface of the dielectric layer through the adhesive layer, using (I) a green sheet roll (3) obtained by winding up the ceramic green sheet (30) having a layer structure comprising a third substrate sheet (31) and the dielectric layer (33) into a roll shape**(see Kuramitsu et al. Para 9; Detailed Description) **; (II) an adhesive layer-forming roll (2) obtained by winding up an adhesive layer-forming sheet (20) having a layer structure comprising a back transfer (offset)-preventing layer (21)** (see Kuramitsu et al. Para35; Detailed Description)**, a second substrate sheet (22) and the adhesive layer (24) into a roll shape; and (III) an electrode layer-forming roll (1) obtained by winding up an electrode sheet (10) having a layer structure comprising a first substrate sheet (11) and an electrode-spacer layer (14) into a roll shape**(see Kuramitsu et al. Para7; Detailed Description) **, said process comprising: (A) a first step of transferring only the adhesive layer (24) of the adhesive layer-forming sheet (20) wound off from the adhesive layer-forming roll (2) onto an upper surface of the dielectric layer (33) of the ceramic green sheet (30), while winding off the ceramic green sheet (30) from the green sheet roll (3); (B) a second step of transferring only the electrode-spacer layer (14) of the electrode sheet (10) wound off from the electrode layer-forming roll (1) onto the adhesive layer (24) transferred onto an upper surface of the ceramic green sheet (30) delivered from the first transfer step; (C) a third step of**

bonding the adhesive layer-forming sheet (20) wound off from the adhesive layer-forming roll (2) onto the electrode-spacer layer (14) transferred onto the upper surface of the ceramic green sheet (30) (see Kuramitsu et al.Para30; Detailed Description & Fig 3) **delivered from the second transfer step, through the adhesive layer (24) of the adhesive layer-forming sheet (20), thereby forming a multilayer sheet (40); and (D) a fourth step of winding up the multilayer sheet (40) delivered from the third step, thereby producing a multilayer sheet roll (4)** (see Kuramitsu et al. Para 31; Detailed Description & Fig 3)**.**

Kuramitsu et al. fail to disclose **an adhesive layer,... (A) a first step of transferring only the adhesive layer (24) of the adhesive layer-forming sheet (20) wound off from the adhesive layer-forming roll (2) onto an upper surface of the dielectric layer (33) of the ceramic green sheet (30).**

However, Kobayashi et al., disclose:

[O027]Next, as shown in drawing 6 and drawing 7, the electrode paste of the internal electrode 18 which makes nickel the main ingredients at a layered product is screen-stenciled on the upper surface of said lower invalid layer 20, After drying, said green sheet 14 laminated via the ** form agent layer 12 and the binder layer 15 on the carrier film 13 was stuck by pressure, it exfoliated from the interface of the account ** type agent layer 12 of back to front and binder layer 15, and the one green sheet 14 was laminated.

It would have been obvious to one with ordinary skill in the art at the time of invention to binding electrode layer with dielectric layer using adhesive layer for

reliable multilayer structure with high adhesive strength to avoid thermal crack as taught by Kobayashi et al.

Kuramitsu et al. together with Kobayashi et al., fail to disclose **a spacer layer with a complementary pattern of the predetermined pattern, which electrode layer and spacer layer are laminated on an upper surface of the dielectric layer through the adhesive layer.**

However, Tokuoka et al. disclose in column 6 paragraph 4:
As shown in FIG. 2A, green internal electrode portions 22 are disposed on a green dielectric layer 21. Moreover, green dielectric portions 23 are disposed to bridge gaps among the green internal electrode portions 22.
It would have been obvious to one with ordinary skill in the art at the time of invention to make electrode spacer layer by forming complimentary pattern for precise flattened surface to avoid piercing of dielectric layer as taught by Tokuoka et al.

6. Regarding claim 3, Kuramitsu et al. disclose:

A process according to claim 1, wherein the electrode sheet (10) (see Kuramitsu et al. Fig 1b) **has a layer structure comprising the first substrate sheet (11)** (see Kuramitsu et al. 10;Fig 1b) **, a release layer (12)** (see Kuramitsu et al. 11;Fig 1b) **and the electrode(**see Kuramitsu et al. 12;Fig 1b)**-spacer layer (14) .**

Kuramitsu et al. together with Kobayashi et al., fail to disclose **spacer layer (14).**

However, Tokuoka et al. disclose in column 6 paragraph 4:

As shown in FIG. 2A, green internal electrode portions 22 are disposed on a green dielectric layer 21. Moreover, green dielectric portions 23 are disposed to bridge gaps among the green internal electrode portions 22.

It would have been obvious to one with ordinary skill in the art at the time of invention to make electrode spacer layer by forming complimentary pattern for precise flattened surface to avoid piercing of dielectric layer as taught by Tokuoka et al.

7. Regarding claim 5, Kuramitsu et al. disclose:

A process according to claim 1 wherein the adhesive layer-forming sheet (20) has a layer structure comprising the back transfer (offset)-preventing layer (21), the second substrate sheet (22), a release layer (23) (see Kuramitsu et al. Para35; Detailed Description) **and the adhesive layer (24).**

Kuramitsu et al fail to disclose **the adhesive layer (24).**

However, Kobayashi et al. disclose:

[0024]1n drawing 2, 13 is a carrier film which makes polyester resin the main ingredients, and the ** form agent layer 12 which makes Si the main ingredients beforehand is formed on this carrier film 13. Apply to the upper surface of said ** form agent layer 12 the binder component which makes poly butyral the main ingredients,dry on it, and the binder layer 15 is formed in it, Said slurry was applied to the upper surface of this binder layer 15 by the doctor blade, it dried on

it, and the ceramic green sheet 14 (henceforth the green sheet 14) before calcination of said ceramic sheet 2 was formed in it.

It would have been obvious to one with ordinary skill in the art at the time of invention to binding electrode layer with dielectric layer using adhesive layer for reliable multilayer structure with high adhesive strength to avoid thermal crack as taught by Kobayashi et al.

8. Regarding claim 6, Kuramitsu et al. disclose:

A process according to claim 1, wherein the ceramic green sheet (30) has a layer structure comprising the third substrate sheet (31) (see Kuramitsu et al. 10Fig 2b)**, a release layer (32)** (see Kuramitsu et al. Fig 1b) **and the dielectric layer (33)** (see Kuramitsu et al. 13; Fig 2b)**.**

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuramitsu et al., JP 2001044064 , in view of Kobayshi et al.,JP 2002343674 and Tokuoka et al. US 6550117 as applied against claim 1 above, further in view of Fukui Y et al., JP 07312326 .

10. Regarding claim 4, Kuramitsu et al. disclose:

A process according to claim 1, wherein the electrode sheet (10) (see Kuramitsu et al. Fig 1b) **has a layer structure comprising the first substrate sheet (11)** (see Kuramitsu et al. 10; Fig 1b)**, the release layer (12)** (see Kuramitsu et al. 11; Fig 1b)**, a print-assisting layer (13) and the electrode** (see Kuramitsu et al. 12; Fig 1b)**-spacer layer (14).**

Kuramitsu et al fail to disclose **spacer layer (14).**

However, Tokuoka et al. disclose in column 6 paragraph 4:

As shown in FIG. 2A, green internal electrode portions 22 are disposed on a green dielectric layer 21. Moreover, green dielectric portions 23 are disposed to bridge gaps among the green internal electrode portions 22.

It would have been obvious to one with ordinary skill in the art at the time of invention to make electrode spacer layer by forming complimentary pattern for precise flattened surface to avoid piercing of dielectric layer as taught by Tokuoka et al.

Kuramitsu et al., Kobayshi et al. and Tokuoka et al. fail together to disclose **a print-assisting layer (13).**

However Fukui Y et al. disclose in paragraph 17 Fig 1:

[0017]Hereafter, a concrete embodiment is described. (Embodiment 1) Drawing 1 is used for below and the 1st embodiment of this invention is described to it. The electrode formative layer which consists of multilayer structure of a functional discrete type where the 1st layer formed the layer 16 only for exfoliation in the coating side of the base film 1, and formed the layer 17 only for electrode pattern formation as the 2nd layer on it is formed, The back change prevention layer 18 is formed in the field by the side of opposite [the] so that the electrode pattern 9 may not re-adhere.

It would have been obvious to one with ordinary skill in the art at the time of invention to manufacture a multilayer electronic device; the steps include

making a multilayer structure by forming an electrode formative layer on top of an exfoliation layer to avoid printing accuracy like blurred, thickness fluctuation, pinhole etc as taught by Fukui Y et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AZM PARVEZ whose telephone number is (571)270-1391. The examiner can normally be reached on M-F 8:30-5:30/ Alt Fri day off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MARVIN LATEEF can be reached on 571-270-1493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AAP
06/09/2009

/Marvin M. Lateef/

Supervisory Patent Examiner, Art Unit 4136